

CLAIMS

- 1 1. A method of forming a semiconductor structure, the method comprising the steps
2 of:
3 providing a substrate having a surface oriented on a first crystal plane that
4 enables subsequent crystal planes for channels to be utilized;
5 forming a first transistor so that a sidewall of a first fin body forms a first channel
6 and so that the sidewall of the first fin body is oriented on a second crystal
7 plane to provide a first carrier mobility; and
8 forming a second transistor so that a sidewall of a second fin body forms a
9 second channel and so that the sidewall of the second fin body is oriented
10 on a third crystal plane to provide a second carrier mobility that is
11 different from the first carrier mobility.
- 1 2. The method of claim 1, wherein the step of providing a substrate comprises the
2 step of providing a silicon substrate having surface oriented on a {110} crystal
3 plane.
- 1 3. The method of claim 1, wherein the step of forming a first transistor comprises
2 the step of forming a first transistor so that the sidewall of the first fin body is
3 oriented on a {n n m} plane and n and m are any integer, wherein the step of
4 forming a second transistor comprises forming a second transistor so that the
5 sidewall of the second fin body is oriented on a {a a b} plane and a and b are any
6 integer such that the {n n m} plane and the {a a b} plane are not equivalent by a
7 symmetry transformation.

- 1 4. The method of claim 1, wherein the step of forming a first transistor comprises
2 the step of forming one of a first p-channel FinFET (PFET) and a first n-channel
3 FinFET (NFET), wherein the step of forming a second transistor comprises the
4 step of forming one of a second PFET and a second NFET.
- 1 5. The method of claim 4, wherein the step of forming one of a first PFET and a
2 first NFET comprises forming one of a first PFET and a first NFET so that the
3 sidewall of the first fin body is oriented on a second crystal plane to provide one
4 of an optimized carrier mobility and a non-optimized carrier mobility, wherein
5 the step of forming one of a second PFET and a second NFET comprises forming
6 one of a second PFET and a second NFET so that the sidewall of the second fin
7 body is oriented on a third crystal plane to provide one of an optimized carrier
8 mobility and a non-optimized carrier mobility.
- 1 6. The method of claim 4, wherein the step of forming one of a first PFET and a
2 first NFET comprises forming one of a first PFET and a first NFET so that the
3 sidewall of the first fin body is oriented on one of a {100} crystal plane, a {110}
4 crystal plane, and a {111} crystal plane, wherein the step of forming one of a
5 second PFET and a second NFET comprises forming one of a second PFET and
6 a second NFET so that the sidewall of the second fin body is oriented on one of a
7 {100} crystal plane, a {110} crystal plane, and a {111} crystal plane.

1 7. A semiconductor structure comprising:
2 a substrate having a surface oriented on a first crystal plane that enables
3 subsequent crystal planes for channels to be utilized;
4 a first transistor having a first fin body, the first fin body having a sidewall
5 forming a first channel, the sidewall of the first fin body oriented on a
6 second crystal plane to provide a first carrier mobility; and
7 a second transistor having a second fin body, the second fin body having a
8 sidewall forming a second channel, the sidewall of the second fin body
9 oriented on a third crystal plane to provide a second carrier mobility that
10 is different from the first carrier mobility.

1 8. The semiconductor structure of claim 7, wherein the silicon substrate surface is
2 oriented on a {110} crystal plane.

1 9. The semiconductor structure of claim 7, wherein the sidewall of the first fin body
2 is oriented on a {n n m} plane and n and m are any integer, wherein the sidewall
3 of the second fin body is oriented on a {a a b} plane and a and b are any integer
4 such that the {n n m} plane and the {a a b} plane are not equivalent by a
5 symmetry transformation.

1 10. The semiconductor structure of claim 7, wherein the first transistor is one of a
2 first p-channel FinFET (PFET) and a first n-channel FinFET (NFET), wherein
3 the second transistor is one of a second PFET and a second NFET.

1 11. The semiconductor structure of claim 8, wherein the sidewall of the first fin body
2 of one of the first PFET and the first NFET is oriented on a second crystal plane
3 to provide one of an optimized carrier mobility and a non-optimized carrier
4 mobility, wherein the sidewall of the second fin body of one of the second PFET
5 and the second NFET is oriented on a third crystal plane to provide one of an
6 optimized carrier mobility and a non-optimized carrier mobility.

1 12. The semiconductor structure of claim 8, wherein the sidewall of the first fin body
2 of one of the first PFET and the first NFET is oriented on one of a {100} crystal
3 plane, a {110} crystal plane, and a {111} crystal plane, wherein the sidewall of
4 the second fin body of one of the second PFET and the second NFET is oriented
5 on one of a {100} crystal plane, a {110} crystal plane, and a {111} crystal plane.

1 13. A semiconductor structure comprising a chip comprising:
2 a first single crystal semiconductor sidewall channel oriented on a first crystal
3 plane; and
4 a second single crystal semiconductor sidewall channel oriented on a second
5 crystal plane different from the first crystal plane;
6 wherein the first crystal plane is not equivalent to the second crystal plane by a
7 symmetry transformation.

1 14. The semiconductor structure of claim 13, wherein a first mobility is associated
2 with the first crystal plane and a second mobility is associated with the second
3 crystal plane, wherein the first mobility is different from the second mobility.

- 1 15. The semiconductor structure of claim 13, wherein the chip has a surface oriented
2 on a {110} crystal plane.
- 1 16. The semiconductor structure of claim 13, wherein the first single crystal
2 semiconductor sidewall channel is part of a first FinFET and the second single
3 crystal semiconductor sidewall channel is part of a second FinFET.
- 1 17. The semiconductor structure of claim 16, wherein the first FinFET is one of a
2 first p-channel FinFET (PFET) and a first n-channel FinFET (NFET), wherein
3 the second FinFET is one of a second PFET and a second NFET.
- 1 18. The semiconductor structure of claim 17, wherein one of the first PFET and the
2 first NFET is oriented on a second crystal plane to provide one of an optimized
3 carrier mobility and a non-optimized carrier mobility, wherein one of the second
4 PFET and the second NFET is oriented on a third crystal plane to provide one of
5 an optimized carrier mobility and a non-optimized carrier mobility.
- 1 19. The semiconductor structure of claim 17, wherein one of the first PFET and the
2 first NFET is oriented on one of a {100} crystal plane, a {110} crystal plane, and
3 a {111} crystal plane, wherein one of the second PFET and the second NFET is
4 oriented on one of a {100} crystal plane, a {110} crystal plane, and a {111}
5 crystal plane.

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